Hardware Upgrade of the L1 Global Muon Trigger in the CMS Experiment at the LHC

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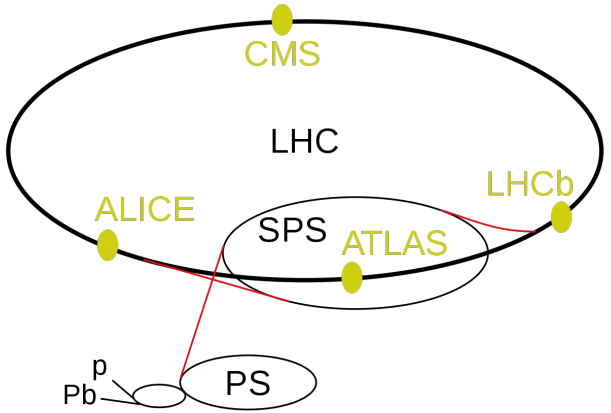
Background: LHC & the Compact Muon Solenoid (CMS) Experiment

The Large Hadron Collider (LHC)

- One of the best tools we have for scientific discovery
- 27 km diameter circular collider located in Swiss-French border near Geneva
- RF cavities accelerate bunches of particles
- Superconducting magnets bend the trajectories and bring bunches to various collision points
- Proton-proton collisions began in 2010 at a center of mass energy of 7 TeV
- Higgs boson discovered in 2012 by CMS, ATLAS collaborations
- Collisions now happen at a center of mass energy of 13.6 TeV, bunch crossing rate of 40MHz

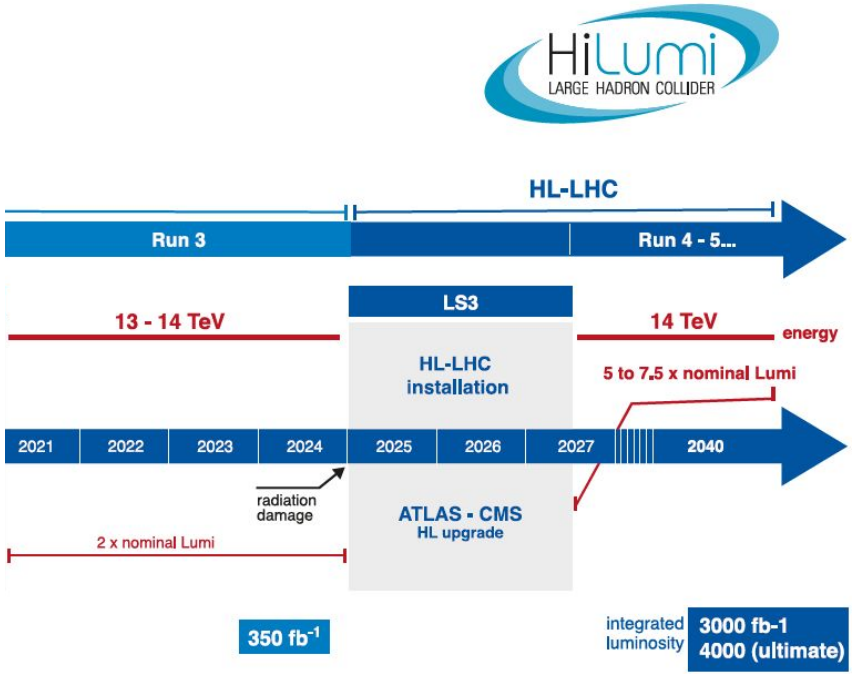


The Large Hadron Collider (LHC)

- Scheduled upgrade in the next couple of years with the aim of increasing the instantaneous luminosity 5 to 10 times nominal value
- Detector upgrades are needed in order to handle the increased luminosity

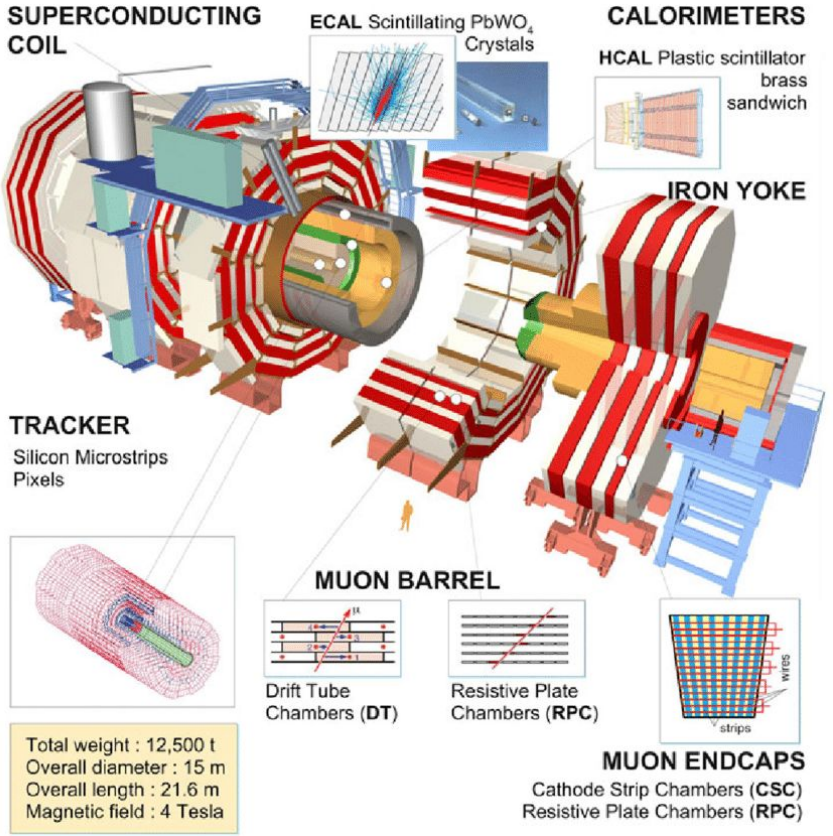
$$\mathcal{L} = f \frac{n_1 n_2}{4\pi\sigma_1\sigma_2}$$

f - Collision frequency
n_1, n_2 - Number of particles
σ_1, σ_2 - Beam parameters



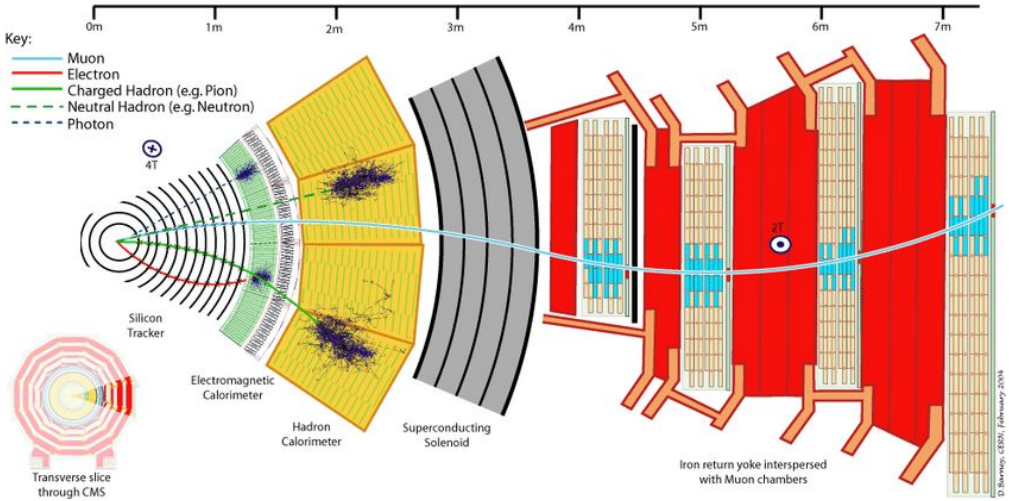
The Compact Muon Solenoid (CMS) Experiment

- One of the general purpose detectors at CERN
- Joint discovery of the Higgs boson in 2012 along with ATLAS collaboration
- Segmented construction with endcap and barrel regions
- Superconducting solenoid
  - 3.8T Magnetic Field
- Inner tracker
- Electromagnetic calorimeter
- Hadronic calorimeter
- Return yoke
- Muon chambers



The Compact Muon Solenoid Experiment(CMS)

- Subsystems designed to measure different types of particle signatures
  - Tracks
  - Energy deposits
- Unrealistic to store each event
  - ~1 petabyte per second
- Sophisticated algorithms select events that may include interesting or rare phenomena

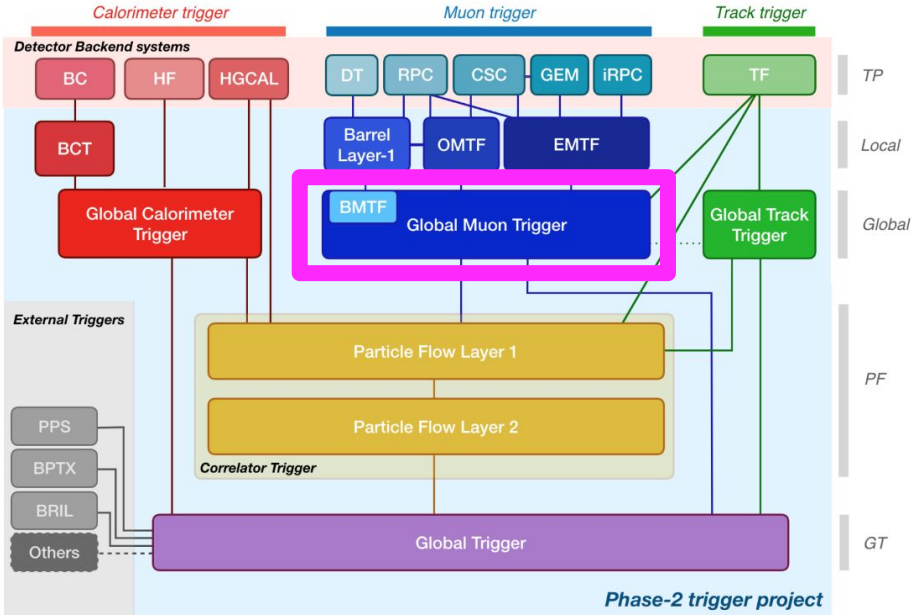


The CMS Trigger System

- Two level trigger system reduces data rate by selecting events of interest
  - **Hardware based level 1(L1) trigger** receives coarse information from detector subsystems & makes quick (few μs) decisions, reducing rate to ~100 kHz
  - Software based high level trigger (HLT) performs more detailed analysis on data passed by L1 trigger - further reducing rate to ~1 kHz
- Data from sub-detectors combined to single event record
- Data stored to disk at CERN's Tier-0 computing center
- Collaborative effort - member institutions contribute to experimental operations

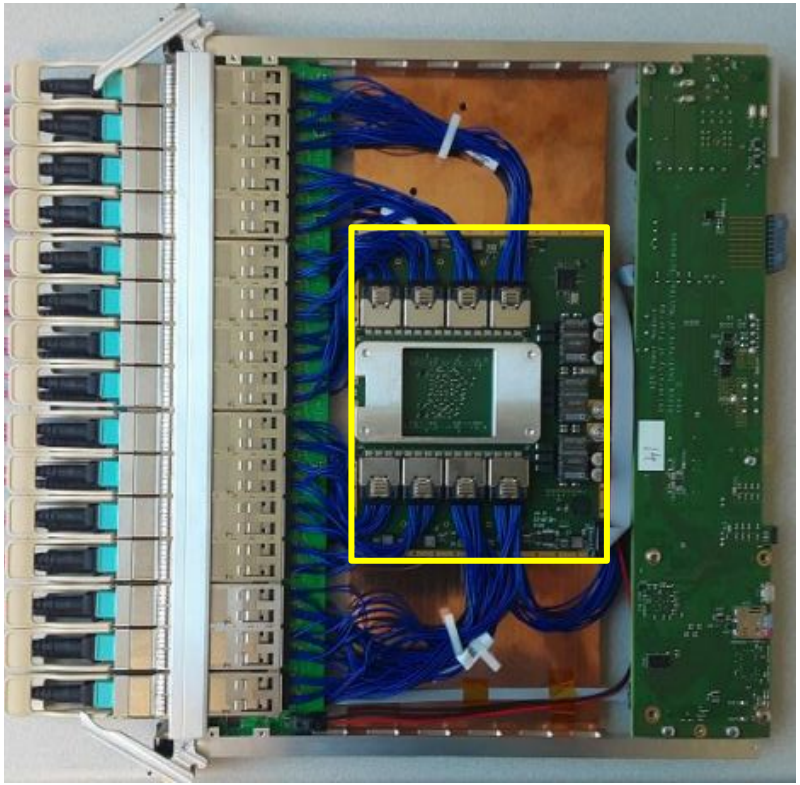
Overview of the Global Muon Trigger(GMT)

- Composed of multiple hardware processing boards
- Receives data from muon detector systems and L1 track trigger
  - Drift Tubes (DT)
  - Resistive Plate Chambers(RPC)
  - Cathode Strip Chambers(CSC)
  - Gas Electron Multipliers (GEM)
- The L1 trigger takes track primitives from the muon stations, tracker and makes muon tracks for entire detector
- **UCLA is responsible for the upgrade to the Global Muon Trigger to be delivered during LS3**



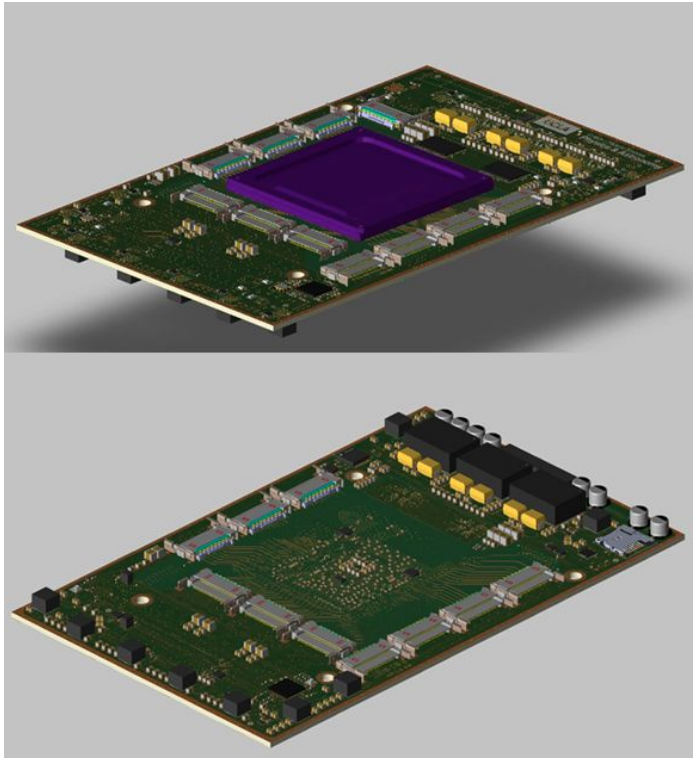
X2O Modular Platform and the Octopus Board

- The processing boards are placed in advanced telecommunications architecture (ATCA) chassis
- The Octopus FPGA module features the VU13P FPGA
- The X2O platform features a large heatsink in which the processing board is placed (center)
- The optical module (left) connects the optical links from the detector to the transceivers which then send signals to the board through twinax cables
- The power module(right) generates the power rails, also features a SOC that performs management and control functions.
- Firmware on FPGA contains the trigger algorithms



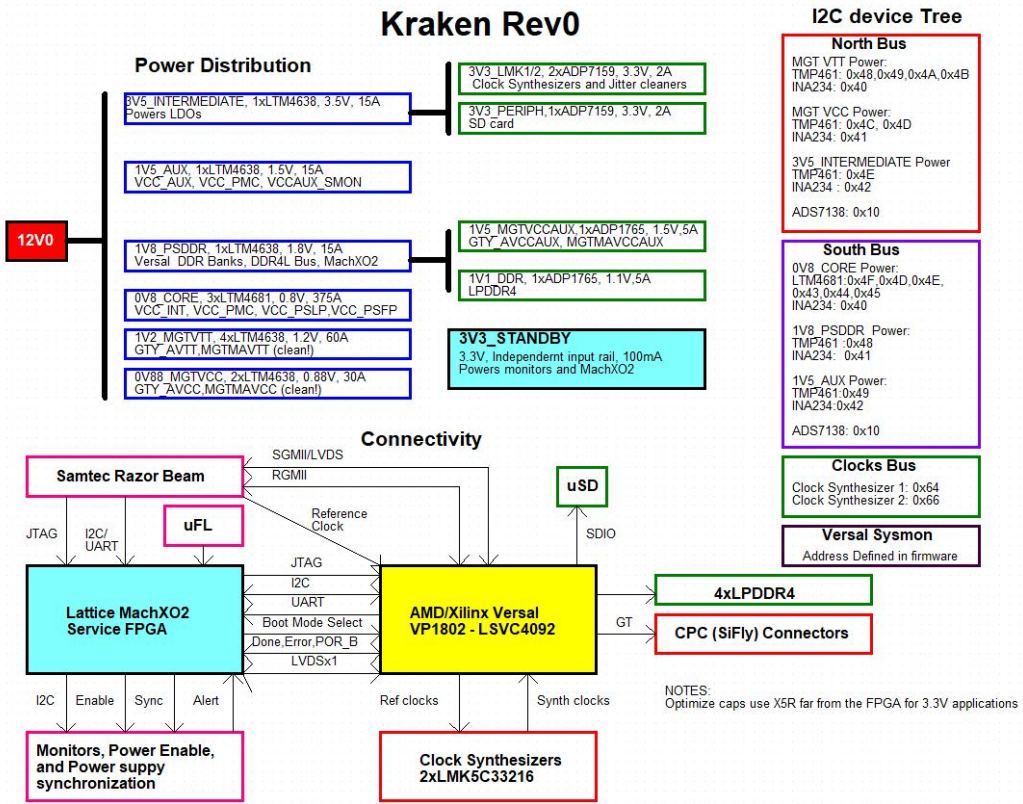
Kraken

- Upgrade of The Octopus FPGA module with next generation 7nm AMD Versal FPGA
- Funding through the HEPCAT fellowship allowed me to contribute to this design by
  - Helping in the schematic and layout design of Kraken
  - Simulating the power supply behaviour for the sensitive electronics and tuning the output filtering capacitance for the power supplies
  - Designing, building, and testing an interface board for Kraken, for power delivery, data transfer, systems monitoring and management



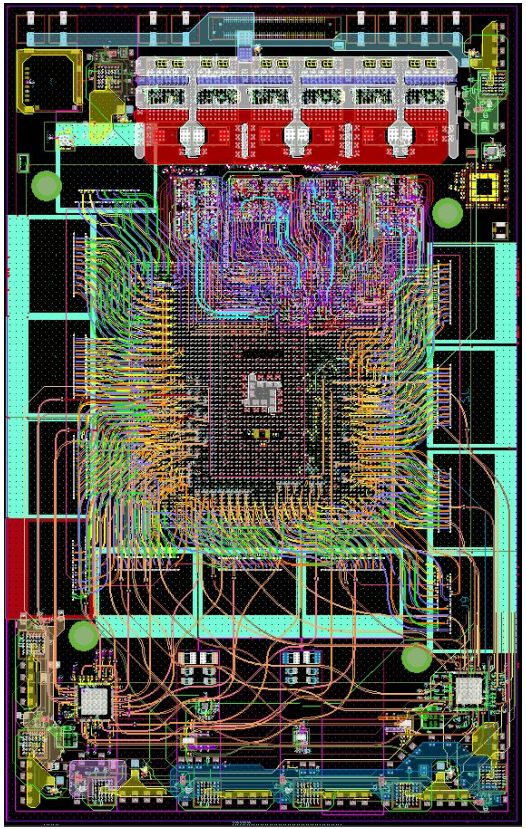
Project: Kraken schematic review

- 70+ pages to review
- Xilinx Versal VP1802 FPGA
  - 140(70) Serial transceivers. Optical links will operate at a nominal 53Gb/s
  - Over 7M logic cells
- 2 LPDDR4 memory controllers (64bit bus size)
- Mach XO2 service FPGA
  - Monitoring,Management
- Power delivery (estimated ~500W)
  - Switching and linear voltage regulators
  - Monitoring ICs
- Clocks, connectors, I2C addresses



Project: Kraken layout and review

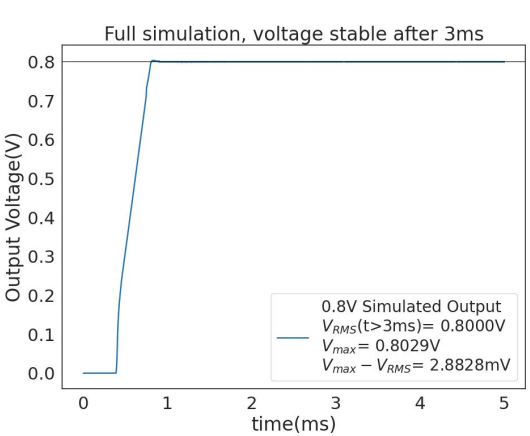
- 18 layer stack up
- High Density Interconnect (HDI) techniques, including use of microvias and buried vias
- Trace and via impedances tuned to differential pair protocols
- Worked in parallel by building sub-modules
- Design completed and reviewed in-house
- First batch of board manufacturing completed and tested with no FPGA → Works
- Board with FPGA expected mid Nov.

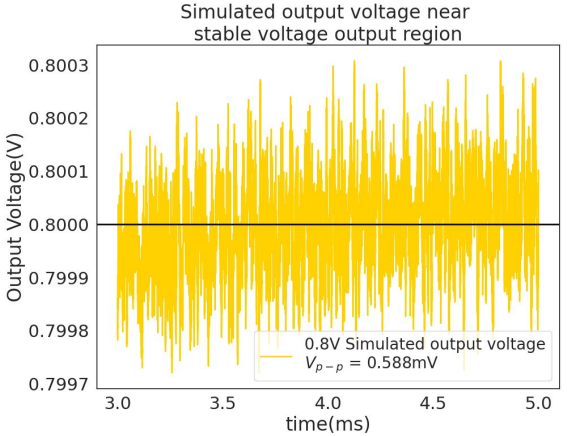


Project: Power supply simulations

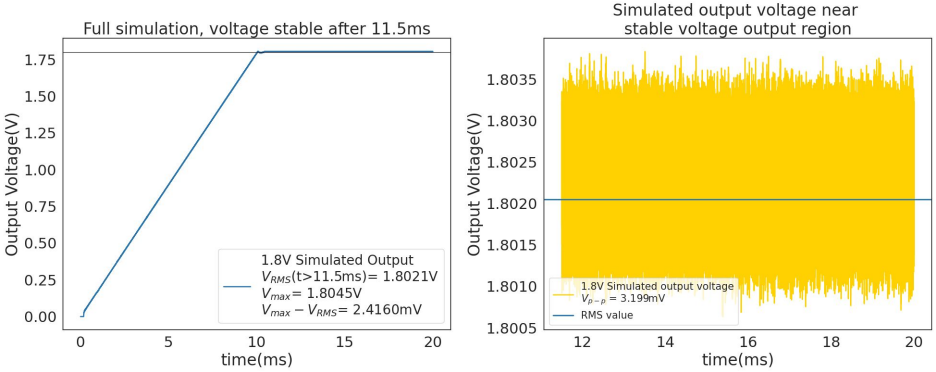
- Kraken will have a core voltage of 0.8V and a current of 375A
- This power rail will be supplied through system of buck regulators stepping down 12V
- LTSPICE Simulations to tune filtering capacitance and to verify ripple voltage would be within acceptable range

LTSPICE simulation of 3 LTM4681s generating 0.8V core voltage at 375A
Load resistor of 2.222$m\Omega$ used, for a simulated current of 360A
9.24mF output filtering capacitance used

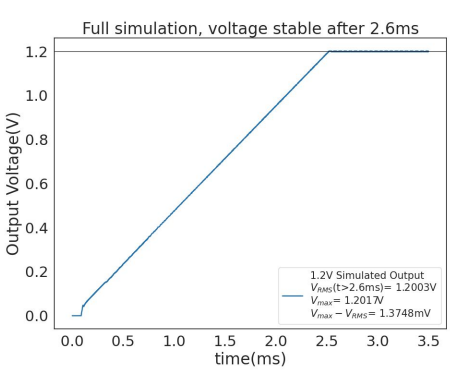


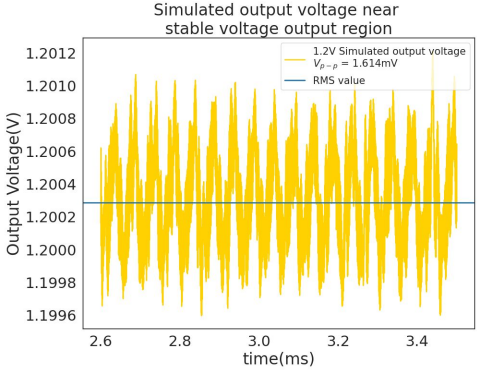


LTSPICE simulation of single LTM4638 generating 1.8V PSDDR voltage at 15A
Load resistor of 138$m\Omega$ used, for a simulated current of 13A
410uF capacitance used. Switching Frequency of 0.998MHz

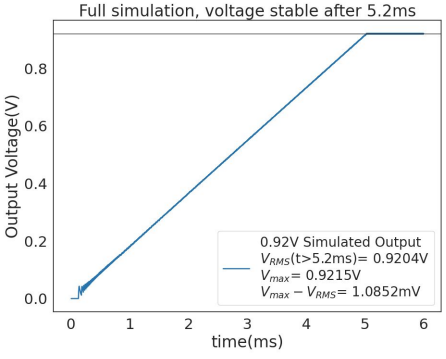


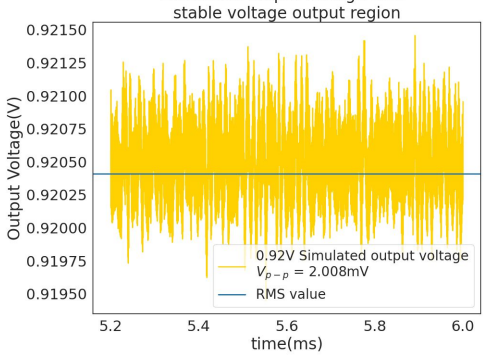
LTSPICE simulation of quad LTM4638s generating 1.2V voltage at 60A
Load resistor of 24$m\Omega$ used, for a simulated current of 50A
1.64mF output filtering capacitance used. Switching frequency of 0.998MHz



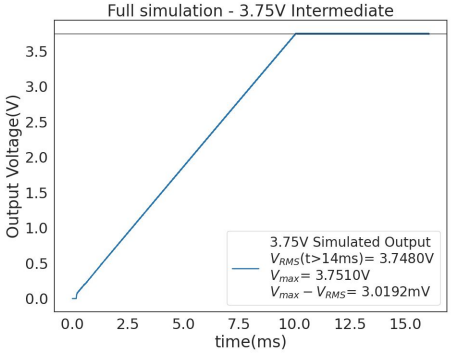


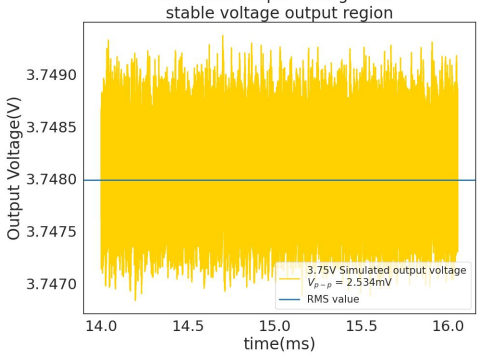
LTSPICE simulation of two LTM4638s generating 0.92V MGTVCC voltage at 30A
Load resistor of 34.1$m\Omega$ used, for a simulated current of 27A
820uF output filtering capacitance used. Switching frequency of 600kHz





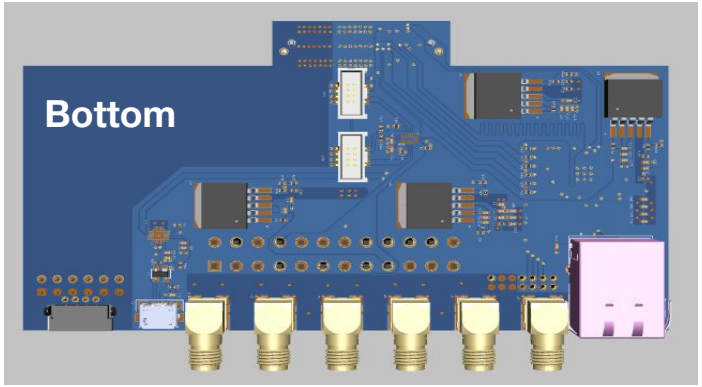
LTSPICE simulation of single LTM4638 generating 3.75V Intermediate voltage at 15A(max)
Load resistor of 269$m\Omega$ used, for a simulated current of 13A
0.410mF output filtering capacitance used

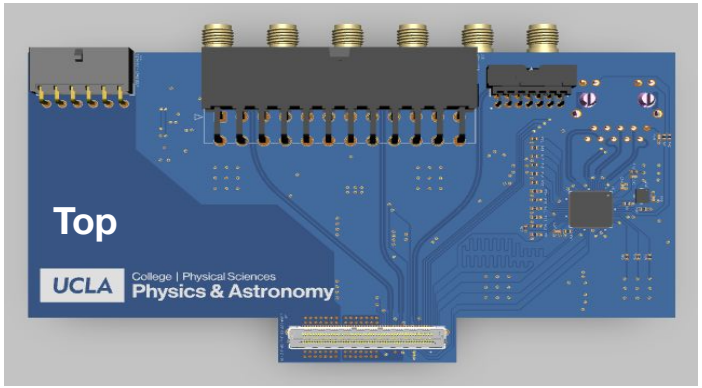




Project: Interface Board

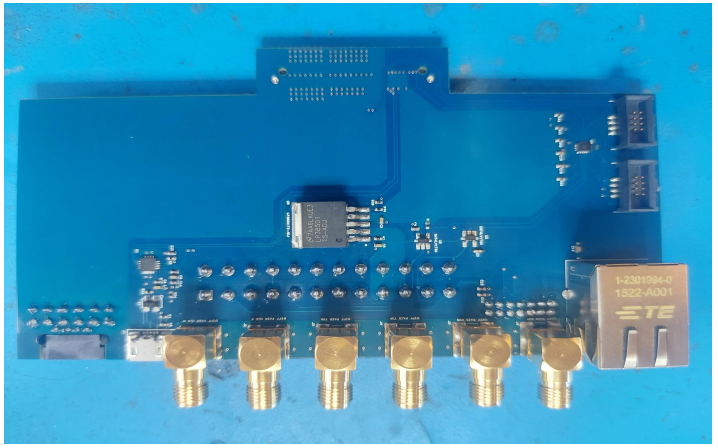
- This board will connect directly to kraken for power delivery, data transfer, systems monitoring and management
- 12V, 3.3V, 5VSB through 24pin ATX Header
  - Will also allow Kraken to function as a CPU
- Dedicated high power connector (NVIDIA 12VHPWR)
- Gigabit ethernet signaling through RJ-45 connector
- Hardware signal protocols: UART, I2C, JTAG, each with dedicated headers
- Differential signaling through SMA connectors (Clocks, Signals)
- Tuned impedance control, 8 layer design
- Connection to kraken through Samtec Razorbeam connector





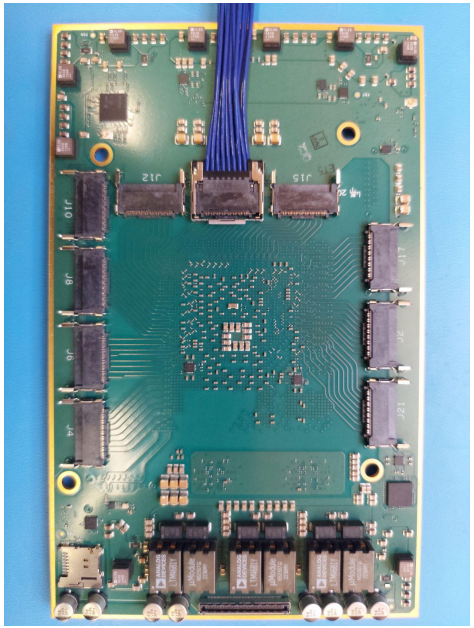
Project: Interface Board

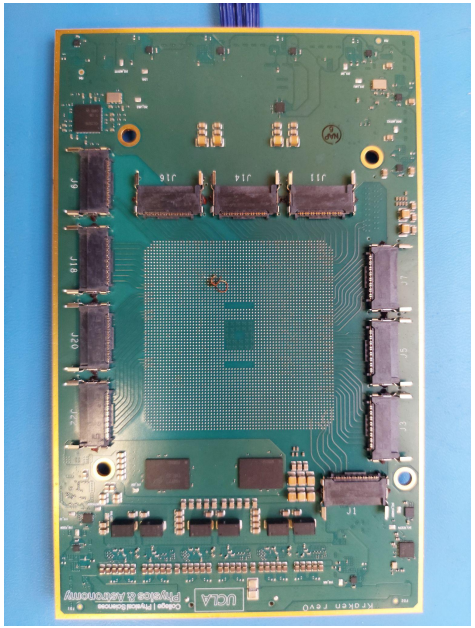
- Ordered 5 PCBs along with ATX power supply
- Assembled at the UCLA electronics shop
- Tested connectivity, standby voltage
- Connected to I2C IO expander through raspberry pi interface
    - Made simple power ON/ OFF and signal readout commands through this interface
- Also tested JTAG, UART

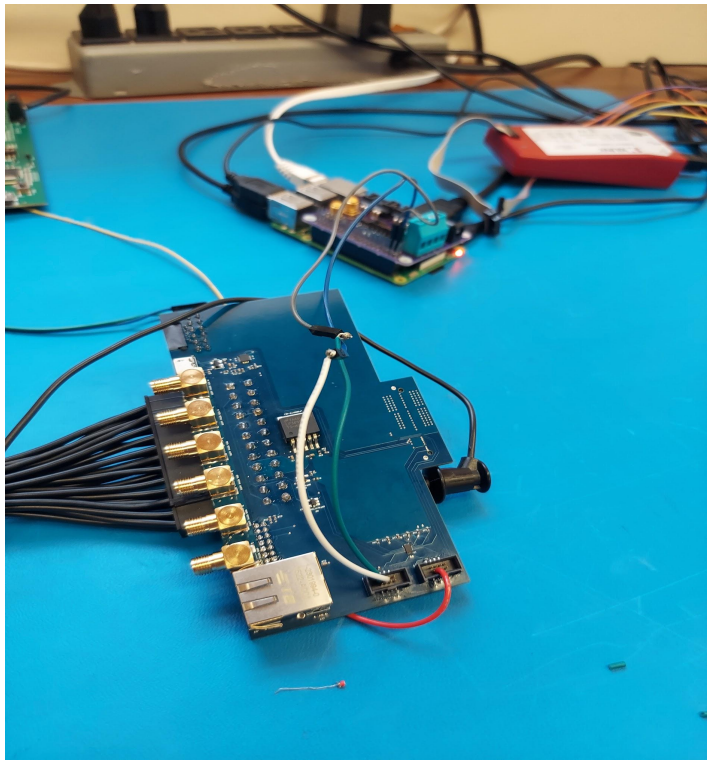


Next Steps

- Kraken PCB assembled
- All components placed on board except for Versal FPGA







Thank You

References

[1] CMS Collaboration (2020) *The Phase-2 Upgrade of the CMS level-1 Trigger* CERN-LHCC- 2020-004 ; CMS-TDR-021. Available at https://cds.cern.ch/record/2714892 [Verified 9 May 2023]

[2] CMS Collaboration (2008) *The CMS Experiment at the CERN LHC* JINST 3 S08004

[3] M.Bachtiset al (2022) *The Octopus processor for the CMS L1 muon trigger for High Luminosity LHC* JINST 17 C03025