The CMS Global Muon Trigger in HL-LHC

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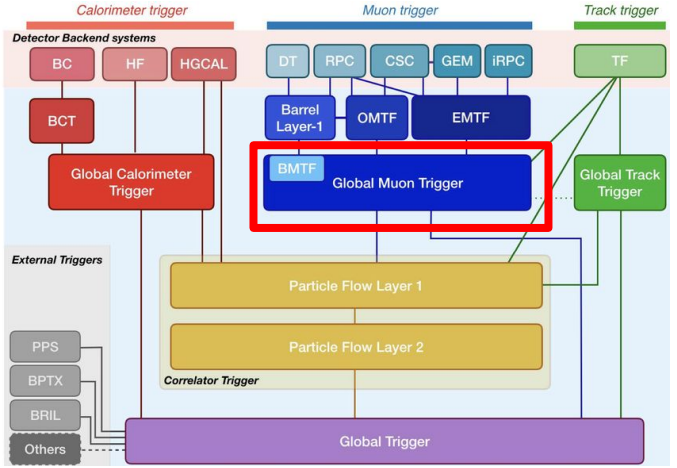
CMS Muon Trigger in HL-LHC

- We need a hardware-based trigger in order to only record interesting events
  - Reduce event rate from 40 MHz to ~1 MHz
- The Level 1 Trigger is the first stage of the overall trigger, and the Global Muon Trigger is a component thereof that reconstructs muons
  - Used in most CMS analyses
- In Phase-2 we can combine silicon tracks and muon station hits to reconstruct “tracker muons” (as opposed to standalone muons which only use muon station hits)
- **My work: Implementation of combined (tracker+muon station) muon reconstruction and implementation of the whole chain in FPGA firmware**



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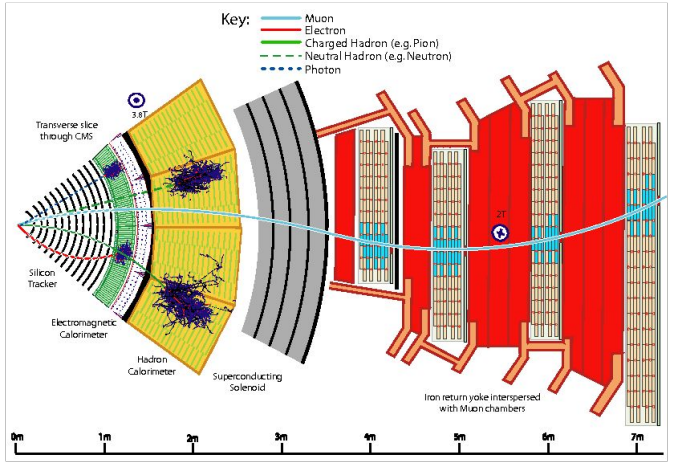
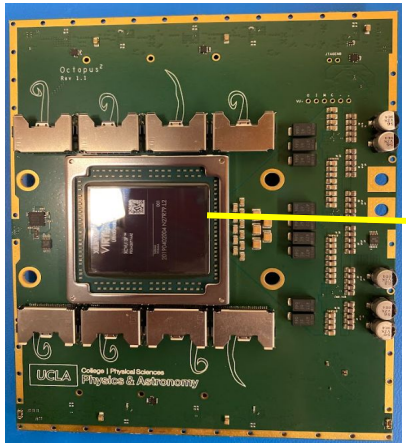


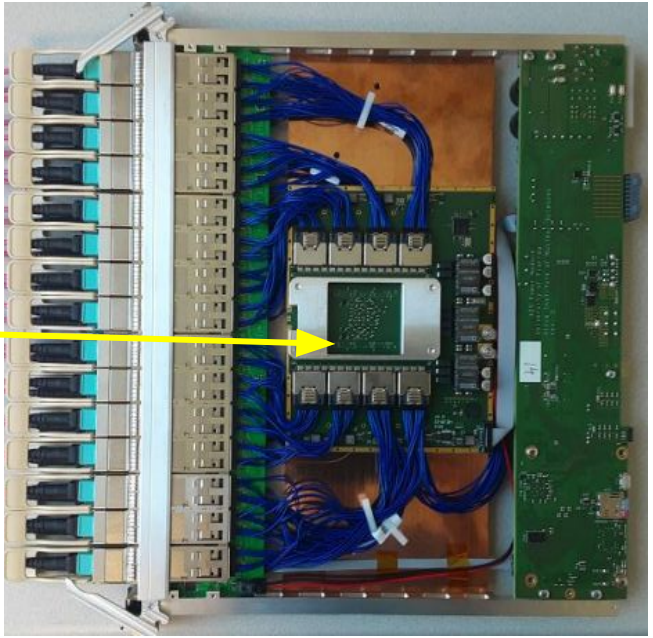
[2]

The X2O board

Modular generic FPGA processor

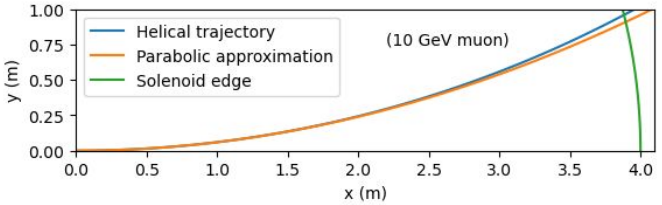
- Large FPGA (AMD/Xilinx VU13P)
- 120 bidirectional optical links
- On board processor and linux system
- 18 X2O boards used in GMT



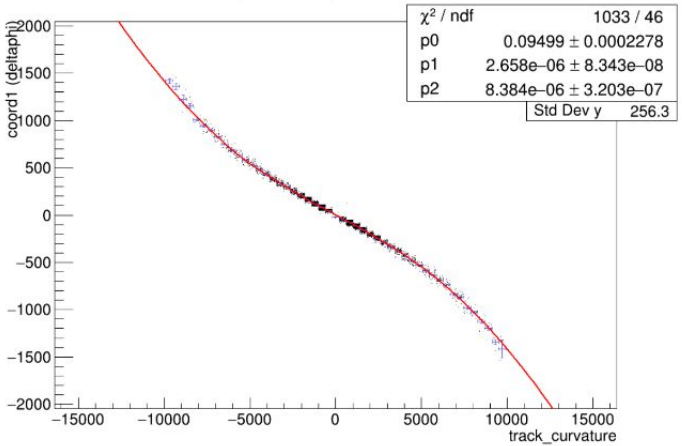


The Tracker Plus Stubs (TPS) Algorithm

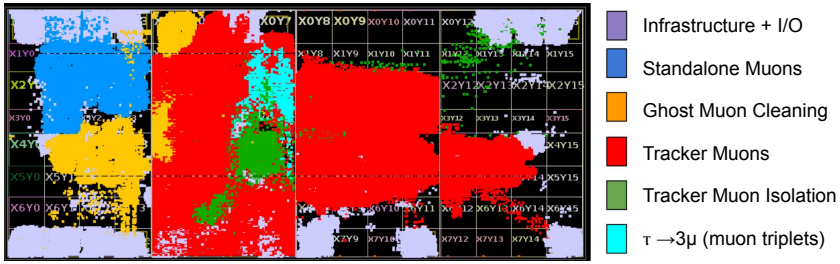
- Propagation of $\Delta\phi$ is due to helical trajectory of charged particles in a magnetic field
  - Approximated as parabolas in the transverse plane
- There is an uncertainty in this propagation from inherent detector resolution and MCS
- We calibrate coefficients used to predict the propagation and uncertainty by matching silicon tracks to muon hits in Monte Carlo events (Drell-Yan and J/Ψ→μμ), calculating the observed propagation, and fitting the result as a function of track curvature (transverse momentum) and pseudorapidity
  - End with LUTs of coefficients used to match tracks to muon hits

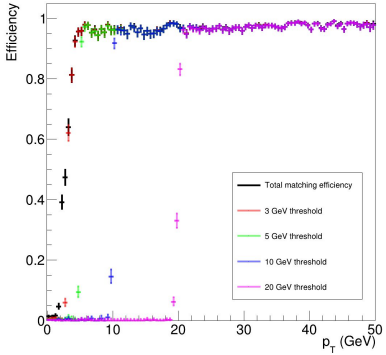


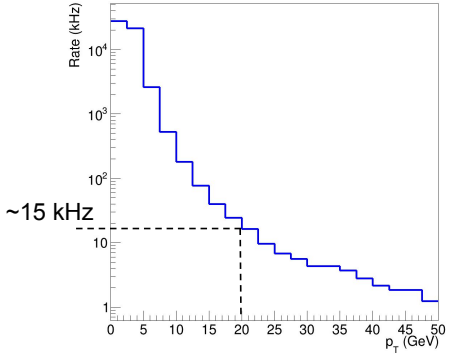
Fit of mean $\Delta\phi$ vs k



Performance and FPGA resources







- Excellent turn on curves and manageable rate at 20 GeV threshold
- Implemented in software emulator and as a pair of High Level Synthesis (HLS) modules in firmware
  - Track matching runs with a latency of 67 ns (24 clock cycles)
  - Cleaning (removing bad matches) runs with a latency of 11 ns (4 clock cycles)

Track matching

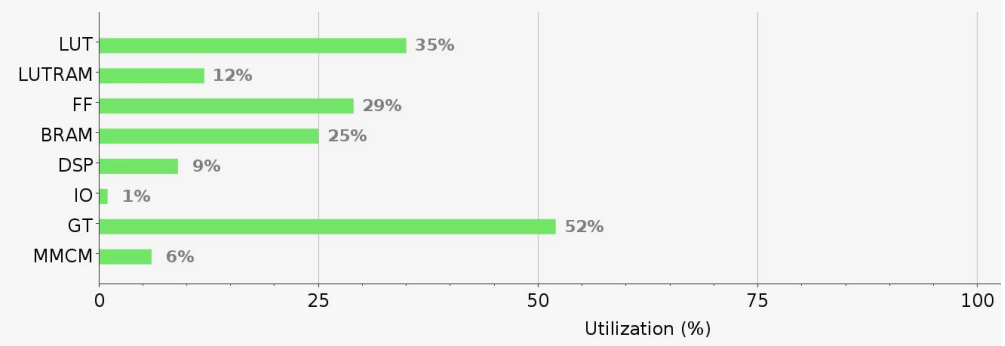
NAME	VERILOG
SLICE	0
LUT	18657
FF	19604
DSP	48
BRAM	49
URAM	0
LATCH	0
SRL	3843
CLB	3822

Cleaning

NAME	VERILOG
SLICE	0
LUT	6546
FF	281
DSP	0
BRAM	0
URAM	0
LATCH	0
SRL	0
CLB	971

PART	FAMILY	PACKAGE	SPEED	LUT	FF	DSP	BRAM
xcvu13p-fsga2577-2-e	Virtex UltraScale+	fsga2577	-2	1728000	3456000	12288	2688

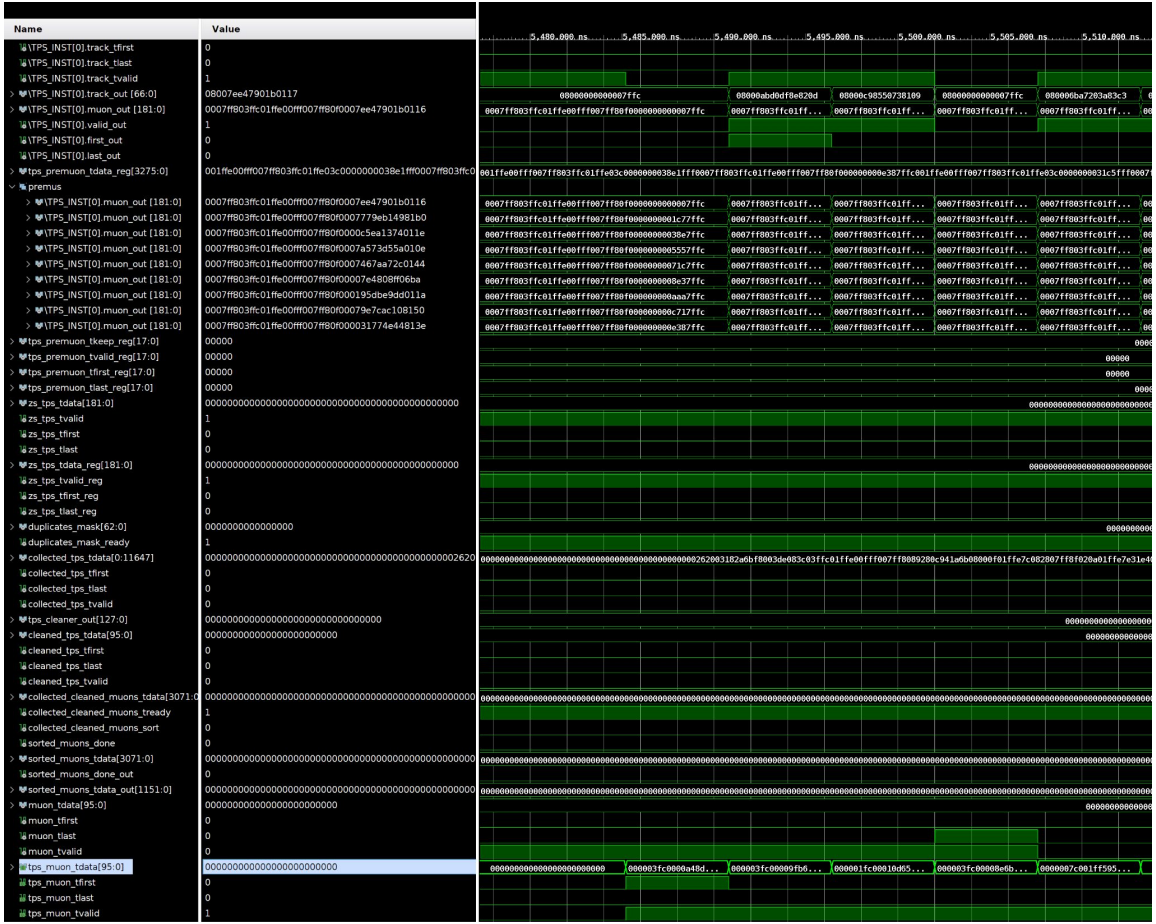
Full GMT Implementation



- TPS Algorithm integrates with the full GMT firmware, running at 360 MHz on X2O board (part xcvu13p-fsga2577-2-e)
  - HLS modules are written and optimized in C++ then synthesized into Verilog
    - These modules are interfaced with the rest of the GMT with several small Verilog modules (deserialization, sorting, duplicate suppression, etc.)
  - Input: serialized streams of pre-processed silicon tracks and muon hits
  - Output: serialized streams of tracker muons sent to the global trigger

Simulation Validation

- Behavioral simulations are run with Vivado and checked against expected results generated from our existing implementation in the software emulator
- Troubleshooting is done with the Vivado Waveform Viewer
  - Lets us see every wire and register at every clock cycle
- Currently have 100% behavioral agreement between emulator and firmware



Future Work

- After full validation of simulation, perform tests on real hardware (X2O board) at UCLA
- Integrate additional algorithms in firmware (muon track isolation, $\tau \rightarrow 3\mu$ reconstruction)
- Perform integration tests with other subsystems using optical connections at CERN

References

- [1] **Particle-flow reconstruction and global event description with the CMS detector** - Sirunyan, A.M. *et al* - arXiv:1706.04965CMS-PRF-14-001CERN-EP-2017-110
- [2] Glazewska, Marianna & Konecki, Marcin. (2022). Level 1 Muon Triggers for the CMS Experiment at the HL-LHC. 1219. 10.22323/1.414.1219.